AU5425: 5 Output Ultra Low Jitter LVCMOS, Fan-Out Buffer

General Description

The AU5425 is a 5 output low-jitter clock, fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution. The low impedance LVCMOS outputs are designed to drive 50 Ω series or parallel terminated transmission lines.

The buffer can choose a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock is distributed to 5 LVCMOS output drivers.

The AU5425 operates from a 3.3 V/2.5 V core supply and 3.3 V/2.5 V output supply. The core supply and output supply are independent of each other and no supply sequencing is required.

Nomenclature:

AU5425: 24 pin, 4 mm x 4 mm, QFN

Applications:

- Carrier Ethernet
- 5G Wireless Infrastructure, Small Cells

Features

- Additive jitter performance of 50 fs RMS.
- Typical output skew between clock outputs is 30 ps
- Level translation with core supply voltage of 3.3 V/2.5 V and 3.3 V/2.5 V / 1.8 V/ 1.5 V output supply for LVCMOS output drivers.
- The device inputs consists of primary, secondary and crystal inputs.
- The inputs are selected by programming input select pins of AU5425. The input clock receiver in AU5425 can accept LVPECL, LVDS, LVCMOS, SSTL, HCSL and OSC waveforms.
- Crystal frequencies from 8 MHz to 50 MHz are supported.
- Crystal input can be over driven with frequency up to 250 MHz in crystal bypass mode
- AU5425 buffer is available in a 24-pin, 4 mm x 4 mm QFN package.

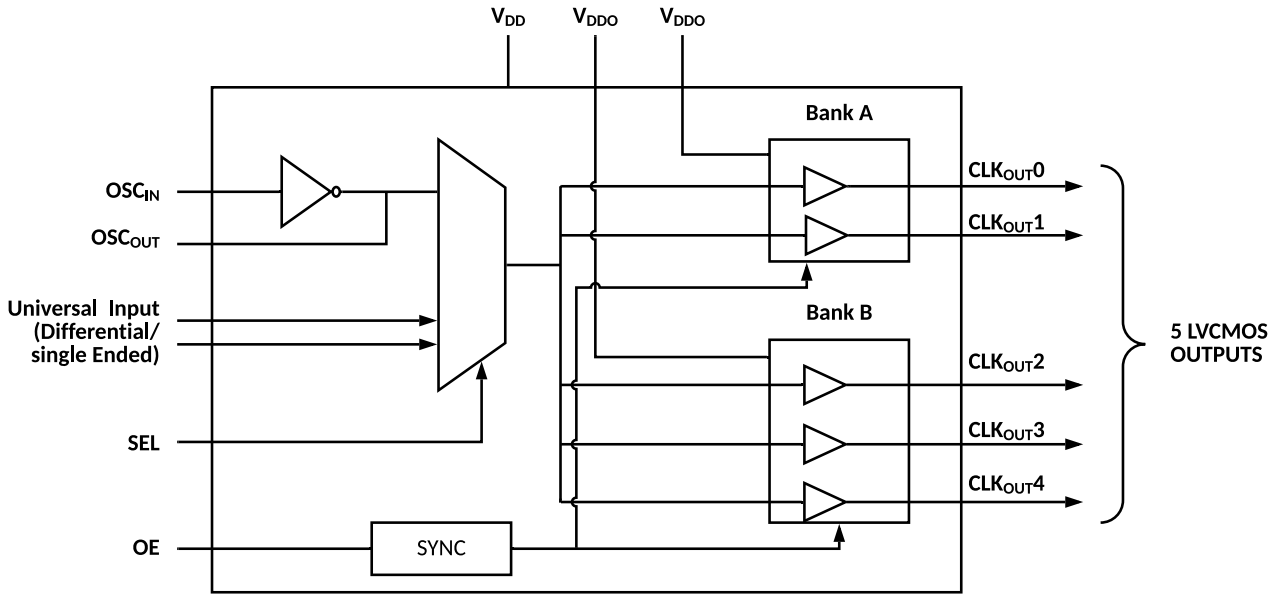

Figure 1 Functional Block Diagram

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1 Detailed Pin Description

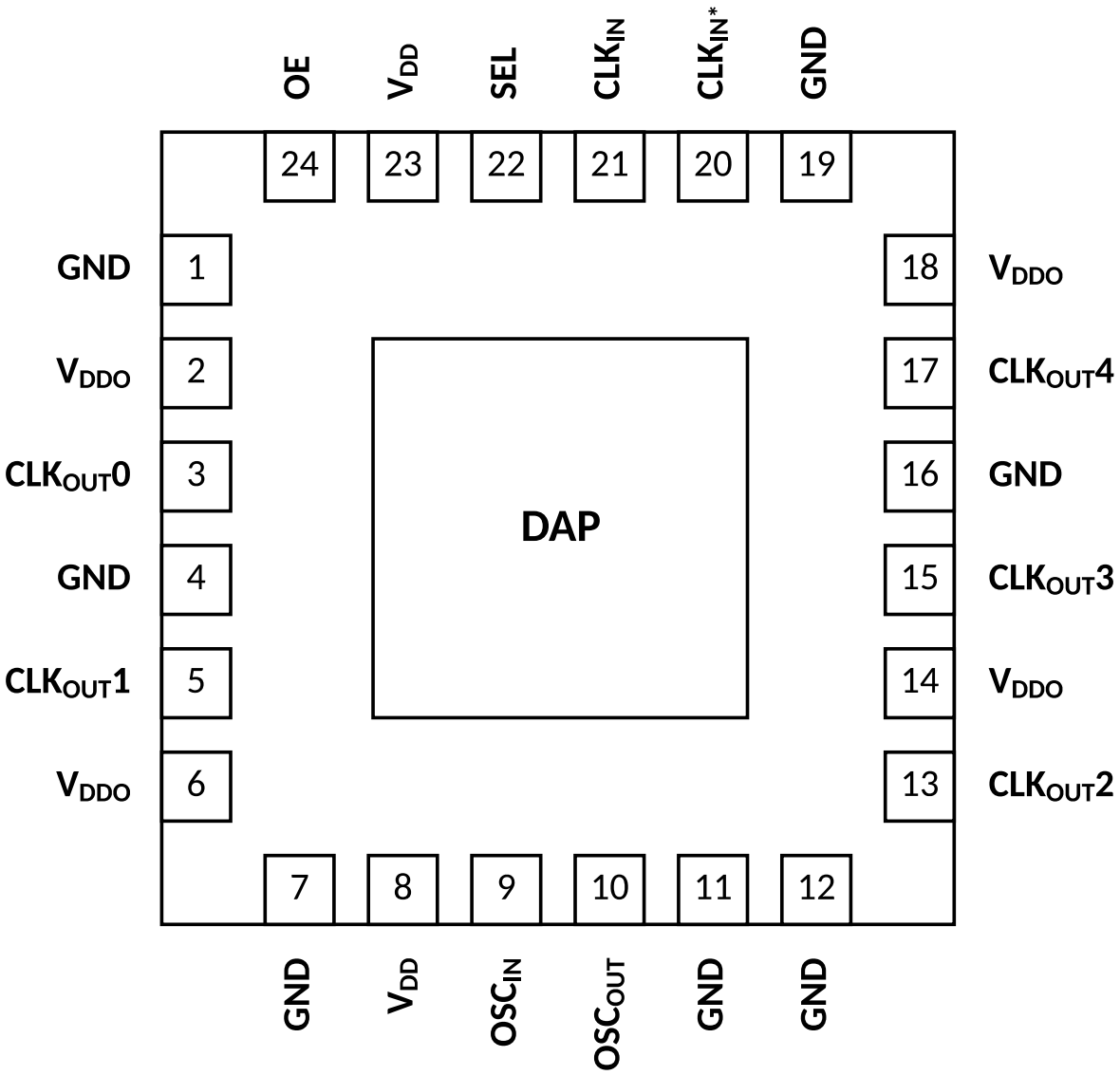


Figure 2 AU5425 Top View

Table 1 Detailed Pin Description

Pin Name	I/O Type	AU5425	Function
DAP	—	DAP	The DAP should be grounded
V_{DDO}	Power	2, 6	Power Supply for Bank A ($CLK_{OUT}0$ and $CLK_{OUT}1$) CLK_{OUT} pins
CLK_{OUT0}	Output	3	LVCMOS Output
GND	GND	1,4,7,11, 12, 16,19	Ground
CLK_{OUT1}	Output	5	LVCMOS Output
V_{DD}	Power	8,23	Supply for operating core and input buffer
OSC_{IN}	Input	9	Input for Crystal
OSC_{OUT}	Output	10	Output for Crystal
CLK_{OUT2}	Output	13	LVCMOS Output
V_{DDO}	Power	14,18	Power Supply for Bank B ($CLK_{OUT}2$ to $CLK_{OUT}4$) CLK_{OUT} pins
CLK_{OUT3}	Output	15	LVCMOS Output

Pin Name	I/O Type	AU5425	Function
CLK_{OUT4}	Output	17	LVCMOS Output
CLK_{IN*}	Input	20	Complementary Input pin
CLK_{IN}	Input	21	Input Pin
SEL	Input	22	Input Clock Selection. This pin has an internal pulldown resistor(1)
OE	Input	24	Output Enable. This pin has an internal pulldown resistor(1)

Notes:

1. CMOS Control Input with Internal Pulldown Resistor

2 Electrical Characteristics

Table 2 Absolute Maximum Ratings

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Absolute Maximum Ratings						
Core Supply Voltage		V_{DD}	-0.5		3.6	V
Output Supply Voltage		V_{DDO}	-0.5		3.6	V
Input voltage, All Inputs, except OSC_IN		V_{IN}	-0.3		VDD+0.3	V
OSC_IN		V_{IN}	-0.3		1.5	V
Storage temperature		T_{STG}	-55		150	°C
Junction Temperature		T_J			125	°C

Notes:

1. Exceeding maximum ratings may shorten the useful life of the device.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 3 Recommended Operating Supply Temperatures

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Ambient Temperature		T_A	-40	27	85	°C
Core Supply Voltage		V_{DD}	3.135	3.3	3.465	V
			2.375	2.5	2.625	V
Output Supply Voltage		V_{DDO}	3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.6	1.8	2	V
			1.35	1.5	1.65	V

Table 4 ESD Ratings

Parameter	Conditions	Symbol	Value	Units
Electrostatic Discharge	Human Body Model		2000	V
	Charged Body Model		500	V

Table 5 Thermal Characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Junction to ambient thermal resistance		θ_{JA}		43.4		°C/W

Table 6 DC Electrical Characteristics

Unless otherwise specified: V_{DD} = 3.3 V ± 5%, 2.5 V ± 5%, V_{DDO} = 3.3 V ± 5%, 2.5 V ± 5%, 1.8 V ± 10%, 1.5 V ± 10%, −40 °C ≤ TA ≤ 85 °C, CLK0/1 driven differentially, input slew rate ≥ 2 V/ns. Typical values represent most likely parametric norms at V_{DD} = 3.3 V, V_{DDO} = 3.3 V, TA = 25 °C.

Parameters	Conditions	Sym	Min	Typ	Max	Units
Current Consumption						
Static current taken by core supply when no toggling	V_{DD} = 3.3 V, V_{DDO} = 3.3 V, F_{IN}= 0	$I_{CORE,STATIC}$		16	19.8	mA

Parameters	Conditions	Sym	Min	Typ	Max	Units
Static current taken by output driver supply when no toggling	V_{DD} = 3.3 V, V_{DDO} = 3.3 V, F_{IN} = 0	$I_{ODR,STATIC}$		3.5	4.2	mA
Current taken by core supply, if OSC is enabled	V_{DD} = 3.3 V, V_{DDO} = 3.3 V, F_{OSC} = 25 MHz	$I_{CORE,STATIC,OSC}$(1)		11.5	14	mA
Power Dissipation Capacitance per output	V_{DD} = 3.3 V, V_{DDO} = 3.3 V, F_{IN} = 200 MHz	C_{PD}(1)		4	5.2	pF
Dynamic current taken by core supply	V_{DD} = 3.3 V, V_{DDO} = 3.3 V, F_{IN} = 100 MHz	$I_{CORE,DYN}$		1.3	1.56	mA
Input Control Pin Characteristics						
High level input voltage		V_{IH}	0.7*V_{DD}		V_{DD}	V
Low level input voltage		V_{IL}	GND		0.3*V_{DD}	V
High level input current	V_{IH} = V_{DD} = 3.3 V	I_{IH}		30	50	uA
Low level input current		I_{IL}	-20	0.1		uA
Pull down resistance		$R_{PULLDOWN}$		200		KΩ
Input capacitance		C_{IN}		2		pF

Notes:

3. Specification is guaranteed by Characterization and not tested in production

Table 7 Digital Inputs (0E, SEL)

Parameter	Conditions	Symbol	Min	Typ	Max	Units
Input Low Voltage		V_{IL}	GND		0.3*VDD	V
Input High Voltage		V_{IH}	0.7*VDD		VDD	V
High Level Input Current	V_{IH} = V_{DD} = 3.3 V	I_{IH}		30	50	uA
Low Level Input Current		I_{IL}	-20	0.1		uA

Table 8 Input Clock Characteristics

Unless otherwise specified: V_{DD} = 3.3 V ± 5%, 2.5 V ± 5%, V_{DDO} = 3.3 V ± 5%, 2.5 V ± 5%, 1.8 V ± 10%, 1.5 V ± 10%, −40 °C ≤ TA ≤ 85 °C, CLK0/1 driven differentially, input slew rate ≥ 2 V/ns. Typical values represent most likely parametric norms at V_{DD} = 3.3 V, V_{DDO} = 3.3 V, TA = 25 °C.

Parameters	Conditions	Sym	Min	Typ	Max	Units
DC Characteristics of universal input clock pins						
High level input current	V_{IH} = V_{DD} = 3.465 V	I_{IH}			650	uA
Low level input current		I_{IL}	-650			uA
Pull up or pull down resistor on CLK0/1		$R_{PULLUP\_PULLDOWN}$		7.5		KΩ
Differential Input Voltage Swing (peak to peak)(1)		V_{IDIFF}	0.15		1.3	V
Differential Input Common Mode Voltage(2)	V_{IDIFF} = 150 mV	V_{ICM}	0.25		V_{DD} – 0.85	V
Single Ended Input High Voltage(2)	Inverting differential input held at VDD/2, V_{DD} = 3.3 V	V_{IHSE}	2		V_{DD}+0.3	V

Parameters	Conditions	Sym	Min	Typ	Max	Units
	Inverting differential input held at VDD/2, V_{DD} = 2.5V		1.6		V_{DD}+0.3	V
Single Ended Input Low Voltage(2)	Inverting differential input held at VDD/2, V_{DD} = 3.3V	V_{ILSE}	-0.3		1.3	V
	Inverting differential input held at VDD/2, V_{DD} = 2.5V		-0.3		0.9	V
AC Characteristics of universal input clock pins						
Input slew rate	20% to 80%	ΔVi/ΔT		2		V/ns
Input Capacitance	Single ended	C_{IN}	—	700	—	fF
Input Frequency Range(4)	LVDS and LVPECL outputs	f_{IN}	—	—	250	MHz
	HCSL outputs		—	—	250	MHz
	LVCMOS outputs		—	—	250	MHz
Input duty cycle, such that output duty cycle is equal to input duty cycle(5)	The pass condition for the measurement is that output duty cycle is within ±5% of input duty cycle. The input clock amplitude is same as LVPECL standard.	I_{DC}	40		60	%
Crystal Characteristics						
Equivalent series resistance		ESR		35	60	Ω
load capacitance		C_L	6	8	10	pF
Shunt Capacitance		C_o		2	3	pF
Drive level				100	200	uW
Mode of oscillation				fundamental		
Supported crystal frequency range(3)		Frequency	8		50	MHz
Maximum swing level on OSC_IN/ OSC_OUT pins	Bypass mode	V_{max}			1.5	V
F_{osc} = 8 MHz	Settling time required for output in crystal mode	t_{settle}		14		ms
F_{osc} = 25, 50 MHz				8		ms
XO bypass AC coupled mode additive jitter(3)	V_{DDO} = 3.3 V Slew Rate > 2 V/ns F_{IN} = 48 MHz	t_{jit}		100		fs
	V_{DDO} = 2.5 V Slew Rate > 2 V/ns Fin = 48 MHz			115		fs
	V_{DDO} = 1.8 V Slew Rate > 2 V/ns F_{IN} = 48 MHz			230		fs
Additive jitter(3)	RMS, integration BW 12 KHz to 5 MHz, $F_{crystal}$ = 25 MHz. Crystal input select Measured at V_{DD} = V_{DDO} = 2.5 V	t_{jit}		155		fs

Notes:

1. Inverting differential input clock pin biased at VDD/2
2. Input common mode defined as VIH.
3. Specification is guaranteed by characterization and is not tested in production

4. If the input clock is initially absent when the chip is just powered up, it will take at least 2 falling edge of clock cycles for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edge of input clock
5. Output duty cycle equals input duty cycle. ATE measurement done with 80% on time and 20% off time waveform to make sure that output duty cycle is equal to input duty cycle even with skewed input duty cycle.

Table 9 Output Clock Characteristics - LVCMOS

Parameters	Conditions	Sym	Min	Typ	Max	Units
Maximum output frequency	Universal clock input	F_{out}			250	MHz
	OSC(1)				50	MHz
Output duty cycle	For $F_{IN} \leq 200$ MHz	Odc	45		55	%
	For 200 MHz < F_{IN}< 250 MHz		40		60	
Output high level voltage	V_{DDO}=3.3 ± 5%, 12 mA pull down current	V_{OH}	2.6			V
	V_{DDO} = 2.5 ± 5%, 8 mA pull down current		1.8			V
	V_{DDO} = 1.8 V ± 200 mV, 2 mA pull down current		1.2			V
	V_{DDO} = 1.5 V ± 150 mV, 2 mA pull down current		0.95			V
Output low level voltage	V_{DDO} = 3.3 ± 5%, 12 mA pull up current	V_{OL}			0.5	V
	V_{DDO} = 2.5 ± 5%, 8 mA pull up current				0.5	V
	V_{DDO} = 1.8 V ± 200 mV, 2 mA pull up current				0.4	V
	V_{DDO} = 1.5 V ± 150 mV, 2mA pull up current				0.35	V
Effective output impedance, for maximum slice strength	V_{DDO} = 3.3 V	R_{out}		15		Ω
	V_{DDO} = 2.5 V			18		Ω
	V_{DDO} = 1.8 V			23		Ω
	V_{DDO} = 1.5 V			28		Ω
Output skew (1)	V_{DDO} = 3.465 V	t_{sk}		40		ps
	V_{DDO} = 2.5V			35		ps
	V_{DDO} = 1.62 V			31		ps
	V_{DDO} = 1.35 V			36		ps
Time for output enable or disable (1)		t_{en}			4	cycle
Input to clock edge to output clock edge delay	V_{DDO} = 3.465 V, PCB trace of 5 inch, 10 pF capacitor AC coupled 50 Ω load	t_d		1.4		ns
	V_{DDO} = 2.5 V, PCB trace of 5 inch, 10 pF capacitor AC coupled 50 Ω load			1.5		ns
	V_{DDO} = 1.62 V, PCB trace of 5 inch, 10 pF capacitor AC coupled 50 Ω load			2		ns
	V_{DDO} = 1.35 V, PCB trace of 5 inch, 10 pF capacitor AC coupled 50 Ω load			2.5		ns
Additive jitter (1)	V_{DDO} = 3.465 V Slew rate (AU5425) ≥ 2 V/ns	t_{jit}		21		fs
	V_{DDO} = 2.5 V Slew rate (AU5425) ≥ 2 V/ns			37		fs
	V_{DDO} = 1.62 V Slew rate (AU5425) ≥ 2 V/ns			87		fs

Parameters	Conditions	Sym	Min	Typ	Max	Units
	V_{DDO} = 1.35 V Slew rate (AU5425) ≥ 2 V/ns			233		fs
Rise time(1)	Output rise time 20% to 80 % Load cap 5 pF, V_{DDO} = 3.3 V, AC coupled 50 Ω load	t_R			605	ps
	Output rise time 20% to 80 % Load cap 5 pF, V_{DDO} = 2.5 V, AC coupled 50 Ω load				605	ps
	Output rise time 20% to 80 % Load cap 5 pF, V_{DDO} = 1.62 V, AC coupled 50 Ω load				605	ps
	Output rise time 20% to 80 % Load cap 5 pF, V_{DDO} = 1.35 V, AC coupled 50 Ω load				605	ps
Fall time(1)	Output fall time 20% to 80 % Load cap 5 pF, V_{DDO} = 3.3 V	t_F			605	ps
	Output fall time 20% to 80 % Load cap 5 pF, V_{DDO} = 2.5 V				605	ps
	Output fall time 20% to 80 % Load cap 5 pF, V_{DDO} = 1.62 V				605	ps
	Output fall time 20% to 80 % Load cap 5 pF, V_{DDO} = 1.35 V				605	ps

Notes:

6. Specification is guaranteed by Characterization and is not tested in production

3 Functional Description

3.1 Functional Block Diagram

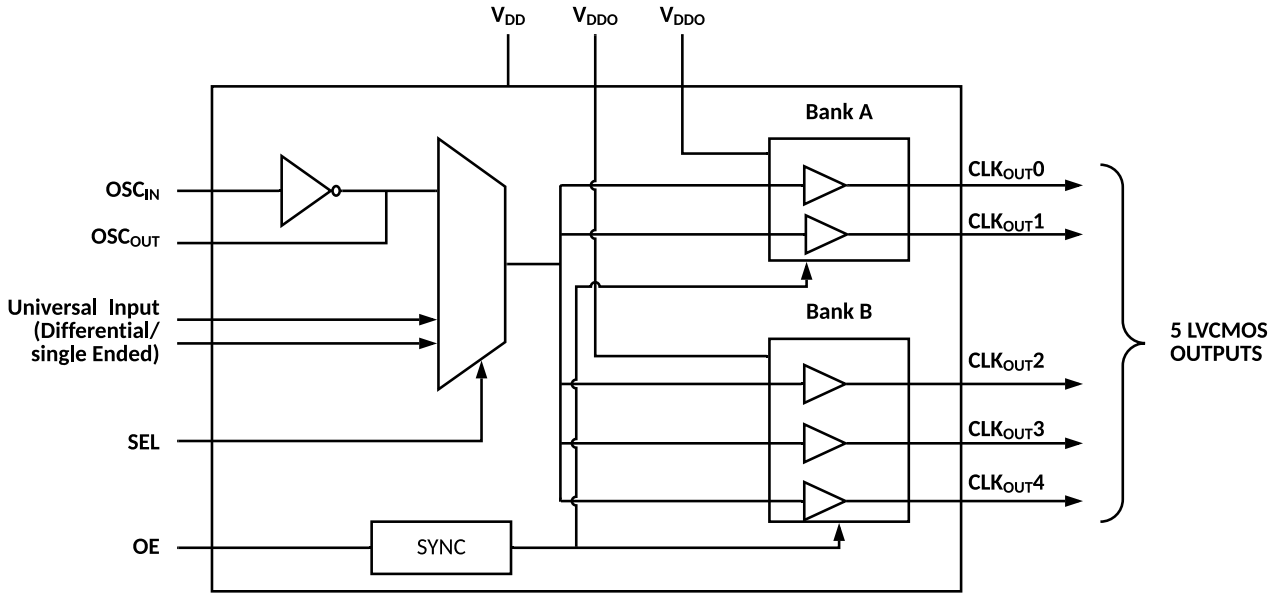


Figure 3 Functional Block Diagram

The AU5425 is a 5-output differential clock fan out buffer with low additive jitter that can operate up to 250 MHz. It features a 2:1 input multiplexer with either a differential/single ended input clock or crystal oscillator input and five LVCMOS outputs. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 24-pin QFN package.

3.2 VDD and VDDO Power Supplies

The AU5425 has separate 3.3 V/2.5 V core (VDD) and 3.3 V/2.5 V/1.8 V/1.5 V output power supply (VDDO). Output supply operation at 2.5 V/1.8 V/1.5 V enables lower power consumption and output-level compatibility with 2.5 V/1.8 V/1.5 V receiver devices. The output levels LVCMOS (VOH) is referenced to its respective VDDO supply.

3.3 Clock Inputs

The input clock can be selected from primary universal clock input, secondary universal clock input, or Xin. Clock input selection is controlled using the SEL[0] inputs as shown in Table 10

Table 10 Input Clock Selection

SEL	Selected Clock
0	CLK
1	Crystal Or Crystal bypass AC coupled mode

3.4 Clock States (Input vs Output States)

Table 11 Input vs Output Stages

State of Selected Clock input	Output State
Inputs are floating	Logic Low
Inputs are logic low	Logic Low
Inputs are logic high	Logic High

3.5 Output Enable

Pulling OE to LOW, forces the outputs to the high-impedance state after the four falling edge of the input signal. The outputs remain in the high-impedance state as long as OE is LOW. The OE signal is internally synchronized to the selected input clock. This allows disabling the output clock at the falling edge of input clock in a glitch free manner.

When OE goes from low to high, the output clock is enabled within a time delay td, where td is given by the following equation.

$t_{d,refout\_en} = 0.5n + 4 * T_{in}$. T_{in} is the time period of the input clock.

Table 12 OE Functionality

OE	Output State
0	Disabled (HIZ)
1	Enabled

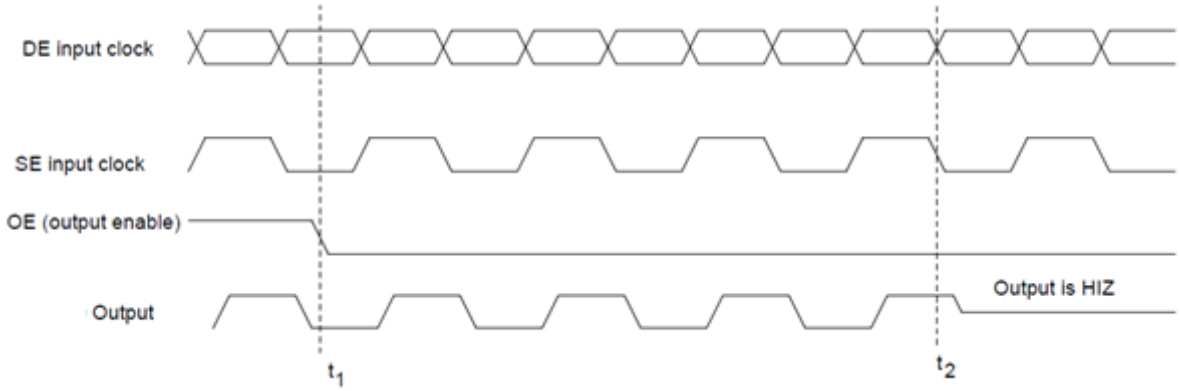


Figure 4 OE: Output Disable (AU5425)

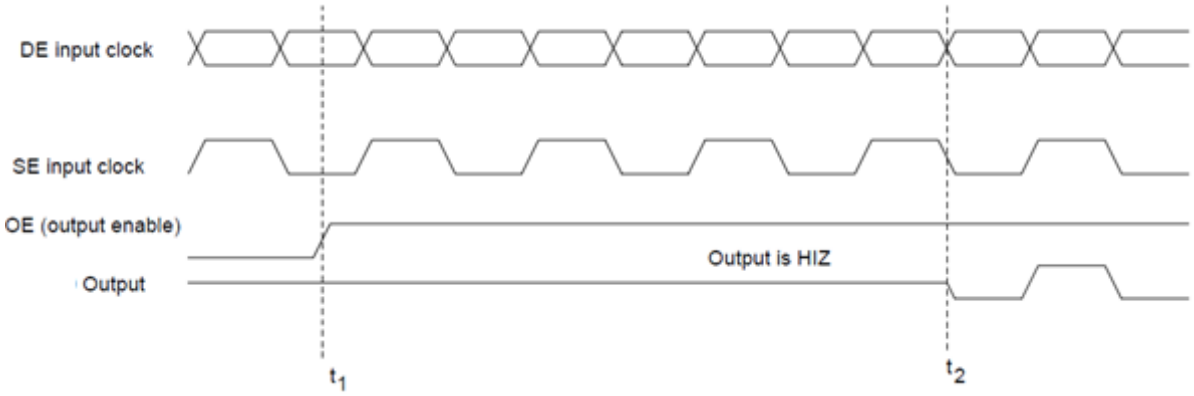


Figure 5 OE: Output Enable

4 Application Information

4.1 Driving the Clock Inputs

The AU5425 has two universal clock inputs (CLK0/nCLK0 and CLK1/nCLK1) AU5425 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The AU5425 supports a wide common mode voltage range and input signal swing

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 2 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter.

It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say CLK0, then nCLK0 pin need to be connected to a 0.1 uF capacitor on the PCB.

4.1.1 Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 6 shows how a differential input can be wired to accept LVCMOS single ended levels in AC coupled mode. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass should be located as close to the input pin as possible. Two resistors R_{T1} and R_{T2} set the common mode voltage at the output of the LVCMOS driver to VDD/2. This prevents average DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{T1} and R_{T2} values should be adjusted to set the V1 at 1.25 V. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

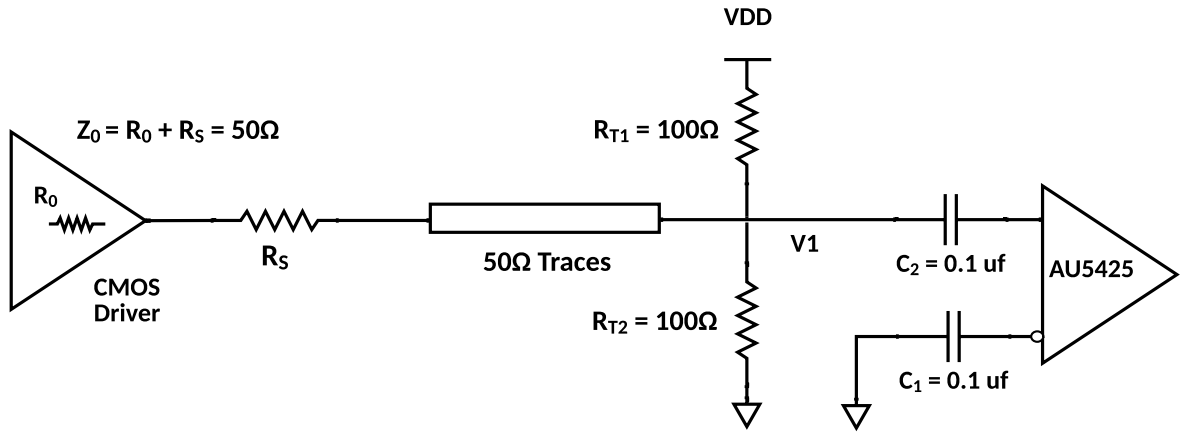


Figure 6 AC coupling LVCMOS clock to AU5425

The inverting differential input can be connected to a 0.1 uF bypass capacitor. This pin is biased internally to a voltage close to VDD/2.

Another variant of the AC coupling of LVCMOS input clock is shown in Figure 7. We use single termination resistor of 50 Ω to ground. A 0.1 uF AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50\ \Omega$$

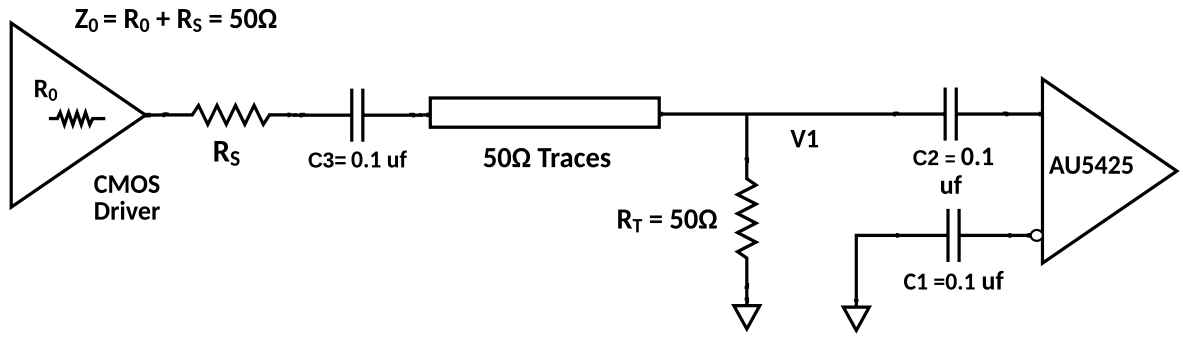


Figure 7 AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

4.1.2 Driving Clock Inputs with LVCMOS Driver (DC coupled)

Figure 8 shows how a differential input can be wired to accept LVCMOS single ended clock signals in DC coupled mode. The reference voltage V1 = VDD/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing. Typical values of bias circuit resistance are R_{S1} = 1 KΩ and R_{S2} = 1 KΩ

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{VDD}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \Omega$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

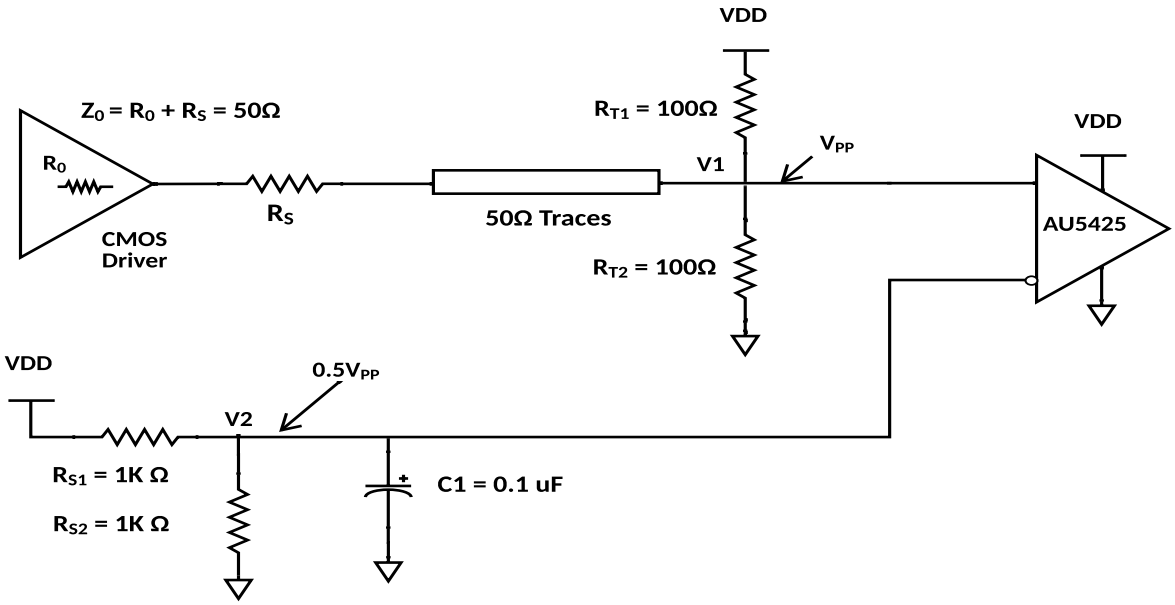


Figure 8 DC coupling of LVCMOS clock to AU5425 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values below are for when both the single ended swing and VDD are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 9 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor RT to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50 Ω load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 9 is given below.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2}$$

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 10. There is a single termination resistor RT which is connected to ground through a capacitor C_{AC}. The value of series capacitor is given by a formula.

$C_{AC} \geq \frac{3T_D}{50\Omega}$ T_D is the transmission line delay

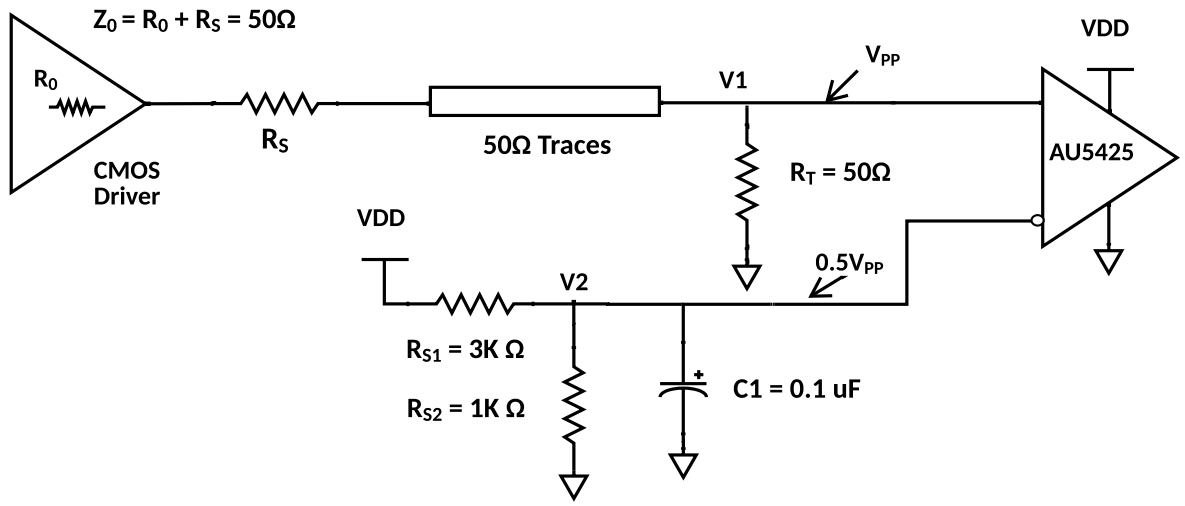


Figure 9 DC coupled LVCMOS input clock configuration – configuration 2

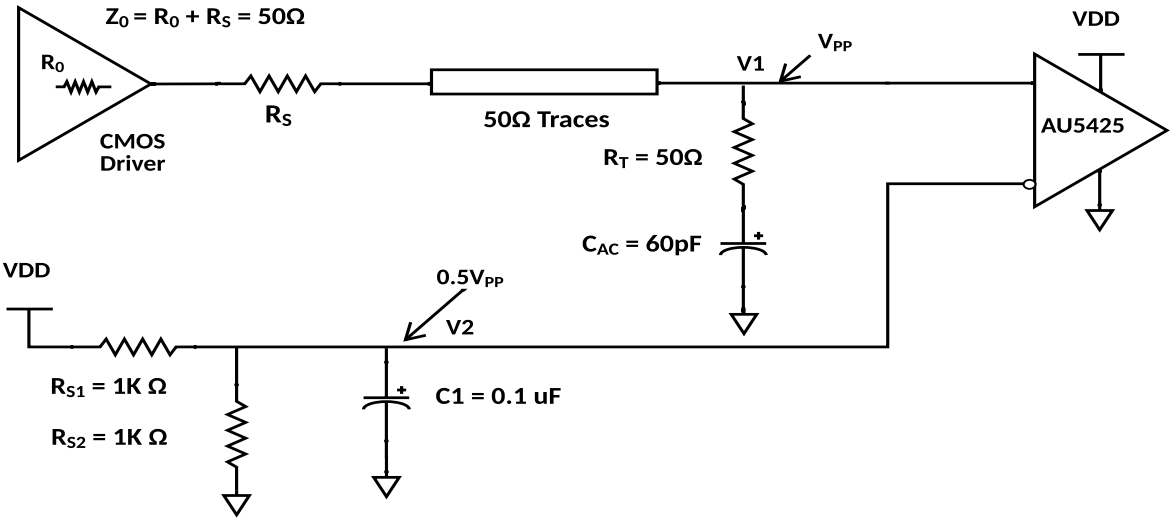


Figure 10 DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can direct couple the LVCMOS clock to AU5425 input clock pin as shown in Figure 11

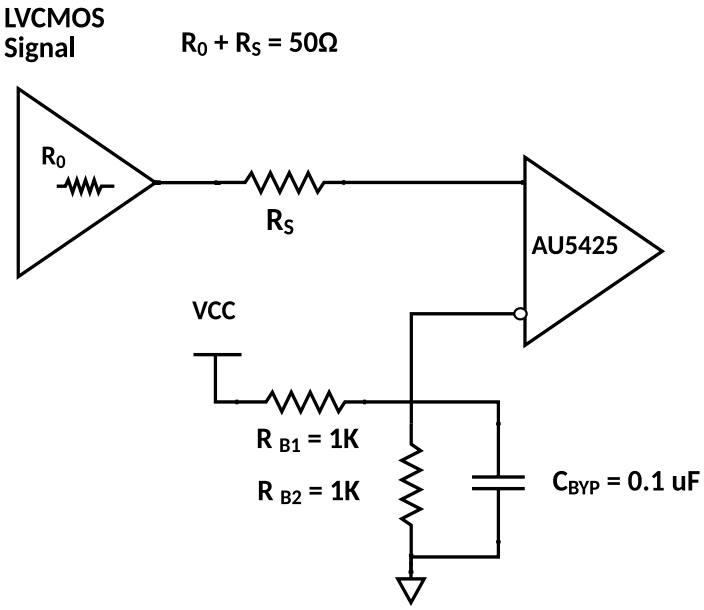


Figure 11: Direct coupling of LVCMOS clock to AU5425

4.1.3 Driving OSC_IN with LVCMOS Driver (AC coupled)

The crystal input OSC_IN can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at OSC_IN should be limited to 1.5 V. The OSC_OUT pin, in this case can be floating. The SEL should be 1. The maximum voltage at OSC_IN should not exceed1.5 V and minimum voltage should not go below -0.3 V. The slew rate at OSC_IN should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 12 shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω.

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.65 V. The maximum DC bias voltage of OSC_IN is 0.675V. Therefore the maximum swing at the OSC_IN pin is given by the equation given below.

$$V_{swing,pk,XTAL\_IN} = 0.675 + 0.5 * 1.65 = 1.5V$$

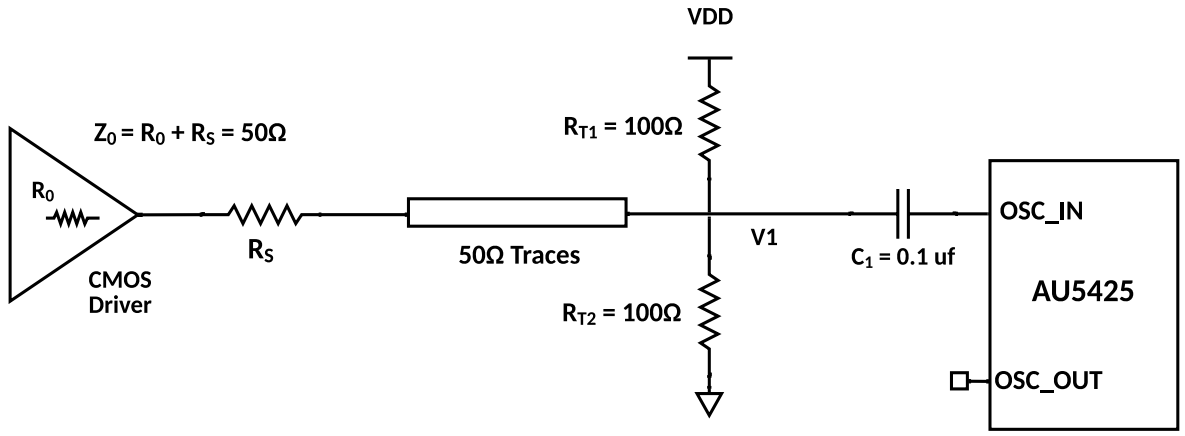


Figure 12 Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 13 shows a second input clock configuration where R_{T1}, R_{T2} are removed and replaced with a 50 Ω termination resistor RT to ground. A 0.1 uF is in series with the CMOS driver to prevent any DC leakage current.

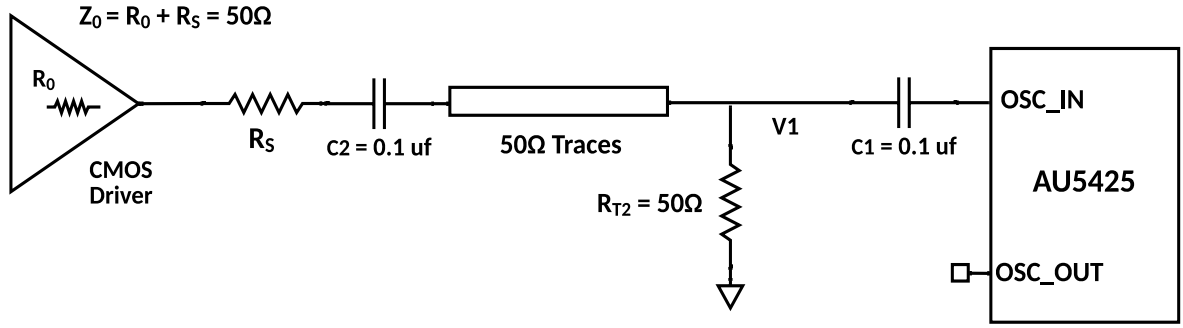


Figure 13 Single ended LVCMOS input – configuration 2, AC coupling to crystal input

4.1.4 LVDS (DC coupled)

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 14

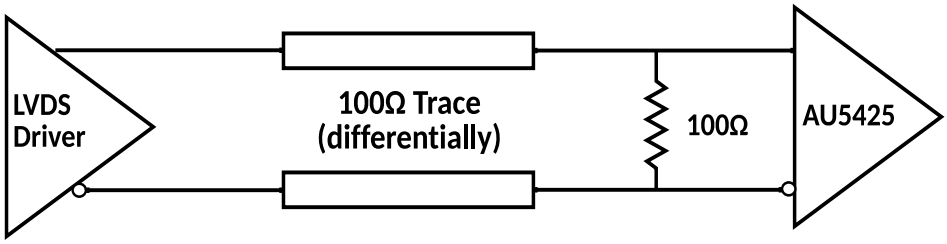


Figure 14 Termination scheme for DC coupled LVDS

4.1.5 HCSL (DC coupled)

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance Rs is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 15

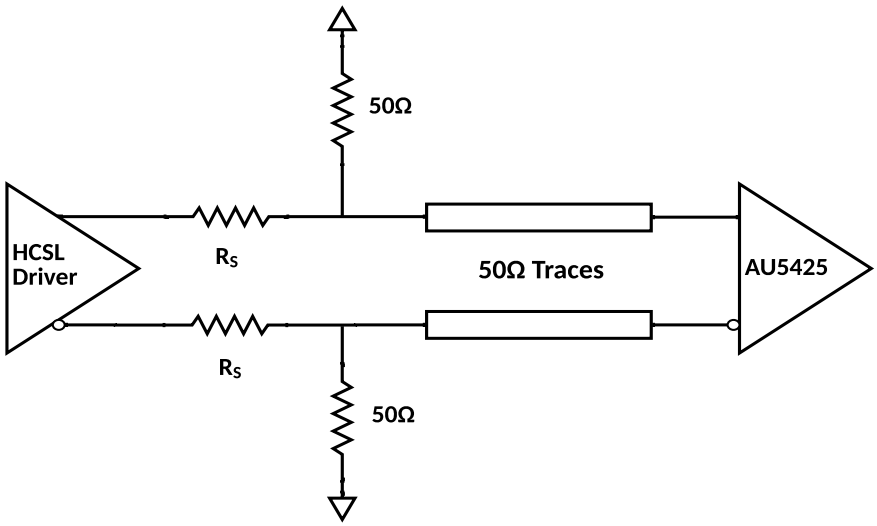


Figure 15 Termination scheme for DC coupled HCSL

4.1.6 LVPECL (DC coupled)

For DC coupled operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source VTT.

$$V_{TT} = V_{DDO} - 2V.$$

This termination scheme is shown in Figure 16. Alternatively, the user can also implement a Thevenin equivalent of VTT using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 17 Termination scheme for DC coupled LVPECL, Thevenin equivalent

.

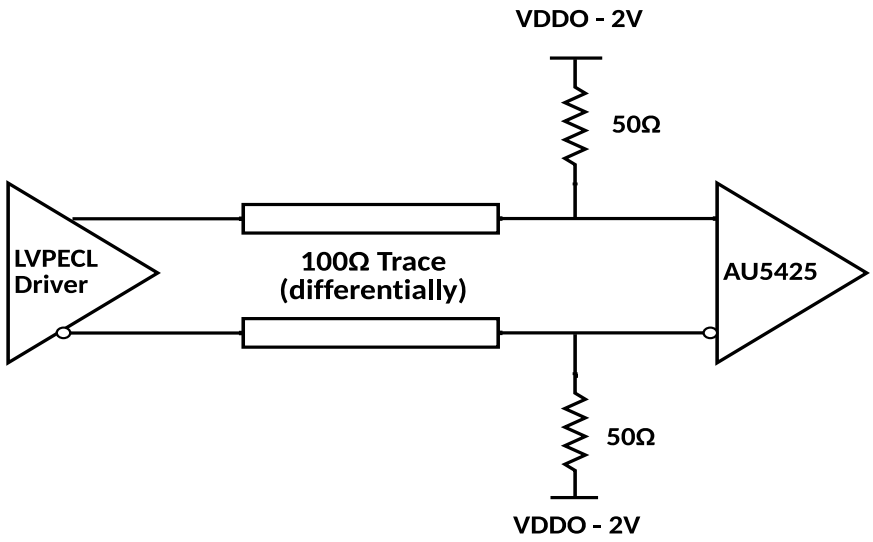
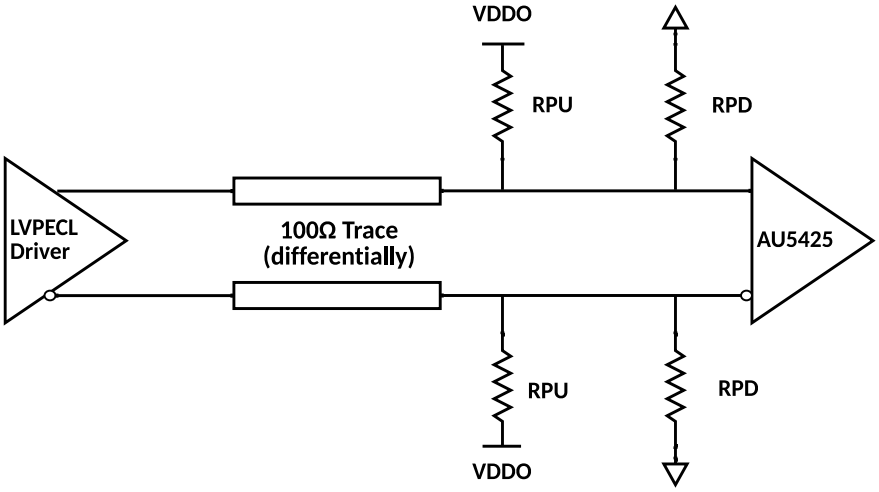


Figure 16 Termination scheme for DC coupled LVPECL



V_{DDO}	RPU	RPD	VTT
3.3 V	120 Ω	82 Ω	~ 1.3 V
2.5 V	250 Ω	62.5 Ω	0.5 V

Figure 17 Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * VDDO}{R_{PD} + R_{PU}} = VDDO - 2V$$

4.1.7 SSTL (DC coupled)

The SSTL input clock configuration is shown in Figure 18. The transmission line impedance is 60 Ω in the application example given. Therefore, we use two 120 Ω resistors from VDDO to ground for biasing the clock input pins. The effective termination impedance in this case is 60 Ω.

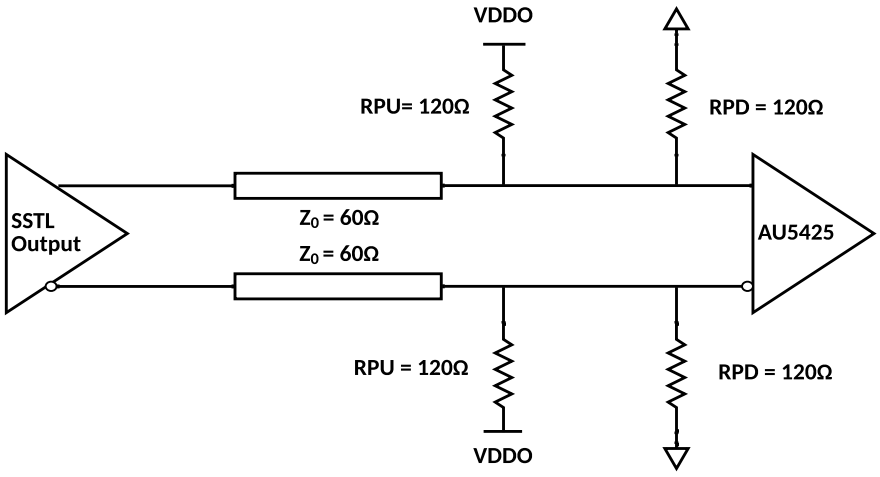


Figure 18 Example of input clock termination for SSTL clock.

4.1.8 LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 19.

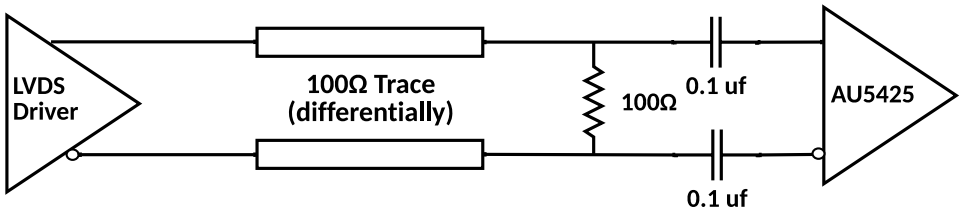


Figure 19 Termination scheme for AC coupled LVDS

4.1.9 LVPECL (AC coupled)

The LVPECL should have a DC path to ground. So, the user must place a resistance R_T, close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 20.

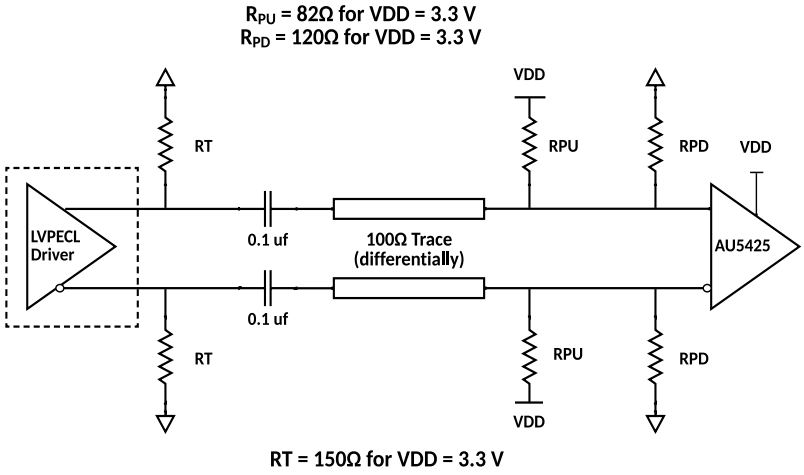


Figure 20 Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance R_{PU} and pull down resistance R_{PD} sets the input common mode voltage for AU5425.

The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{VDD * R_{PD}}{R_{PU+R_{PD}}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The differential input common mode specification of AU5425 (from data sheet) is VDD -1.1 = 2.2 V, therefore the input common mode set by LVPECL AC coupled termination meets the AU5425 input common mode specification.

The LVPECL driver chip has resistance RT providing DC path for the output driver current in the LVPECL driver.

The effective load impedance at the input side of AU5425 (receiver side) is formed by parallel combination of R_{PU}, R_{PD}.

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

4.2 Termination of Output Driver of AU5425 for Various Load Configurations

4.2.1 AU5425 Output ODR Termination for AC Coupled mode

AC coupling of AU5425 LVCMOS output driver is shown in Figure 21. We use single termination resistor of 50 Ωs to ground. A 0.1 uF AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single 50 Ω resistance to ground. The clock signal is then AC coupled to the receiver, in this example. C1 is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50\ \Omega$$

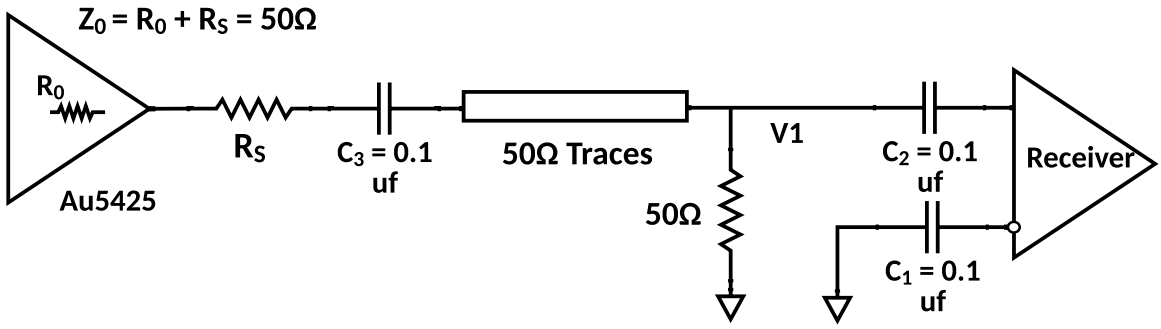


Figure 21 AC coupling of LVCMOS clock with single 50 Ω resistor termination to ground

4.2.2 AU5425 Output ODR Termination for DC Coupled mode

Figure 22 shows how AU5425 LVCMOS output drive can be terminated to send clock signals in DC coupled mode. The reference voltage V1= VDD/2 is generated by the bias resistors R_{S1} and R_{S2}. The bypass capacitor (C_1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R_{S1} and R_{S2} might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ \Omega$$

$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{VDD}{2}, Typical\ value\ of\ R_{s1} = R_{s2} = 1K\Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ Ohm, Typical\ value\ of\ R_{T1} = R_{T2} = 100\Omega$$

$$\frac{VDD * R_{T2}}{R_{T1} + R_{T2}} = \frac{VDD}{2}$$

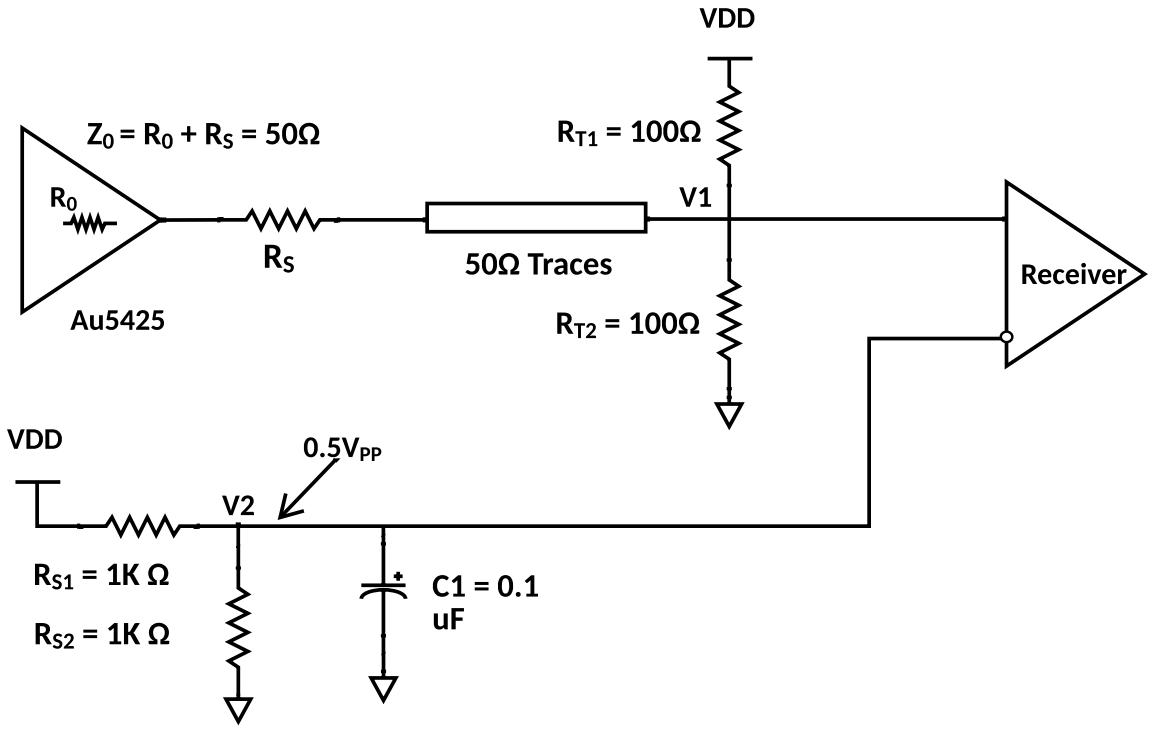


Figure 22 DC coupling of LVCMOS output clock termination – configuration 1

For example, if the AU5425 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the R_{S1} and R_{S2} values should be adjusted to set the V2 at 1.25 V. The values below are for when both the single ended swing and VDD are at the same voltage.

This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R_{T1} and R_{T2} in parallel should equal the transmission line impedance. For most 50 Ω applications, R_{T1} and R_{T2} can be 100 Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 23 shows a second input clock configuration where RT1, RT2 are removed and replaced with a 50 Ω termination resistor RT to ground. There will be DC leakage current from AU5425, for the output termination shown in Figure 23

The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 23

$$Z_o = R_o + R_s = 50\ Ohm$$

$$\frac{VDD * R_{s2}}{R_{s1} + R_{s2}} = \frac{Vpp}{2} = \frac{VDD}{4}, Typical\ value\ of\ R_{s1} = 3K\Omega, R_{s2} = 1K\Omega$$

The AU5425 LVCMOS output driver termination with series RC termination near the buffer is shown in Figure 24. There is a single termination resistor RT which is connected to ground through a capacitor CAC. The value of series capacitor is given by a formula.

$C_{AC} \geq \frac{3T_D}{50\Omega}$, T_D is the transmission line delay

Typical value for C_{AC} is 60 pF, assuming delay of T_D = 200 ps/inch and 5 inch input clock route length.

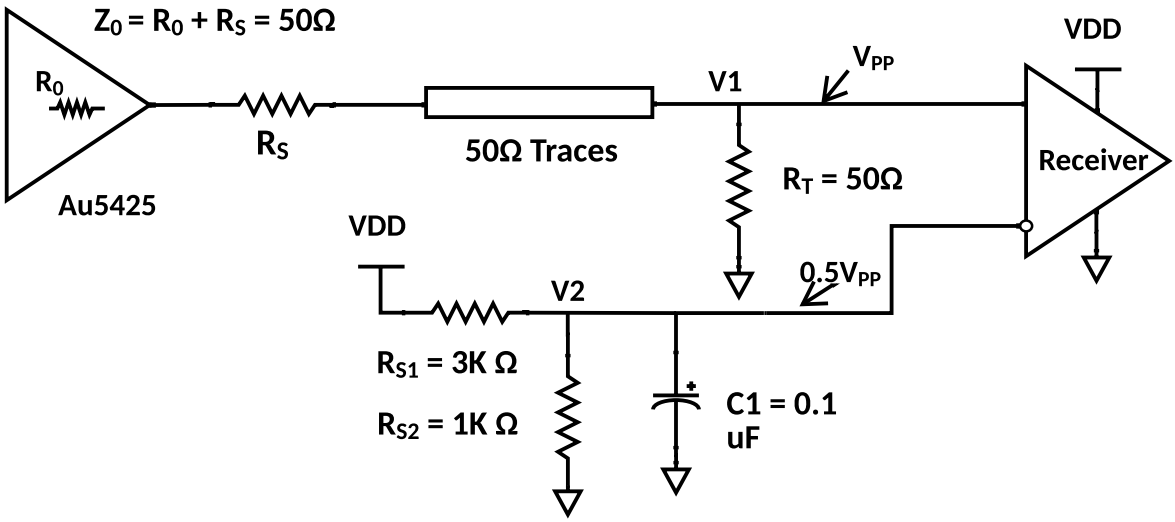


Figure 23 DC coupled LVCMOS output clock configuration – configuration 2

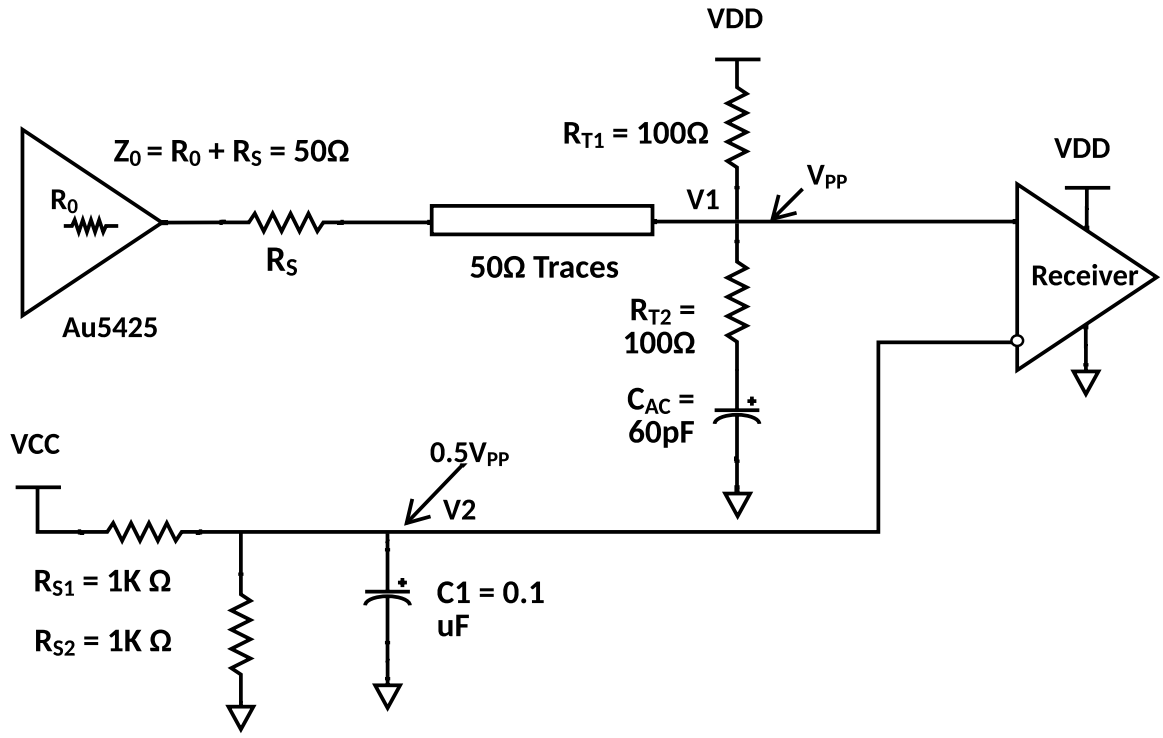


Figure 24 DC coupled LVCMOS output clock with series RC termination – configuration 3

The typical value of R_{S1} and R_{S2} in this case is 1 KΩ and that of C_{AC} is 60 pF.

4.2.3 CMOS (Capacitive load)

The capacitive load can be driven as shown in Figure 25. Rs = 33 Ω for VDDO = 3.3 V.

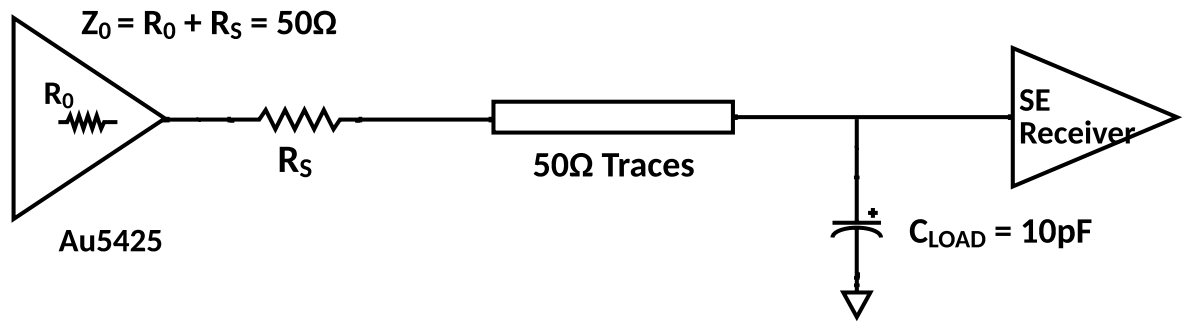


Figure 25 Typical application load

4.3 Power Considerations

The following power consideration refers to the device-consumed power consumption only. The device power consumption is the sum of static power and dynamic power. The dynamic power usage consists of two components:

Power used by the device as it switches states

Power required to charge any output load. The output load can be capacitive-only or capacitive and resistive. Use the following formula to calculate the power consumption of the device:

$$P_{DEV} = P_{STATIC} + P_{DYNAMIC} + P_{CLOAD}$$

$$P_{STATIC} = I_{CORE\_STATIC} * VDD + I_{ODR,\_STATIC} * VDDO$$

$$P_{DYNAMIC} = I_{CORE\_DYNAMIC\_100MHZ} * VDD * \frac{F_{in}(units\ in\ MHz)}{100} + C_{PD} * 5 * F_{in} * VDDO^2$$

$$P_{CLOAD} = C_{LOAD} * 5 * F_{in} * VDDO^2$$

Let us calculate typical power dissipation for C_{LOAD} of 2 pF at input clock of 100 MHZ. Assume that VDD = VDDO = 3.3 V.

$$P_{STATIC} = 16mA * 3.3V + 3.5mA * 3.3V = 64.35mW$$

$$P_{DYNAMIC} = 1.5mA * \frac{100}{100} * 3.3V + 4.0pF * 5 * 100MHz * 3.3V * 3.3V = 26.73\ mW$$

$$P_{CLOAD} = 2pF * 5 * 100MHz * 3.3V * 3.3V = 10.89mW$$

$$P_{DEV} = 102mW$$

4.4 Core Current in XO Mode

The crystal mode standalone block current is measured in ATE. We can calculate total VDD core current in crystal mode, in typical condition using the below equation. The worst case VDD core current will be 14 mA, in crystal mode.

$$I_{core\_crystal} = 8.5 + I_{xo\_standalone} = 11.5mA, typical$$

4.5 Parameter Measurement Information

4.5.1 Differential Input Level

The parameter definitions related to differential input level is shown in Figure 26.

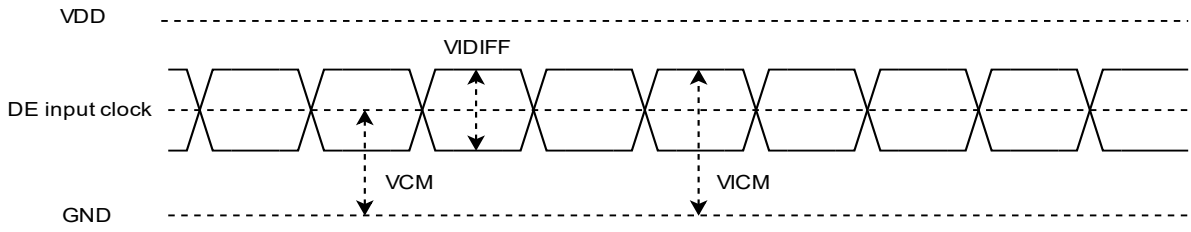


Figure 26 Parameters related to differential input level

4.5.2 Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown in Figure 27

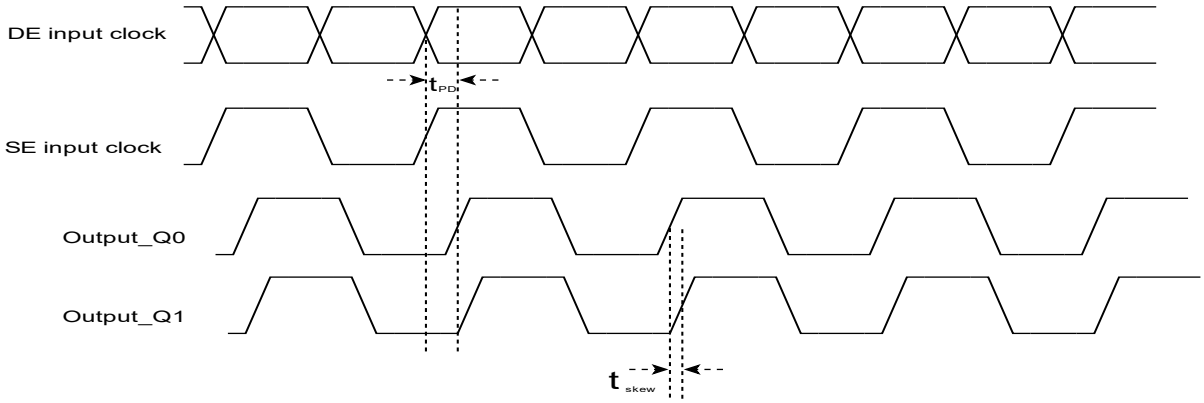


Figure 27 Parameter definitions of propagation delay and skew

4.5.3 Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown in Figure 28.

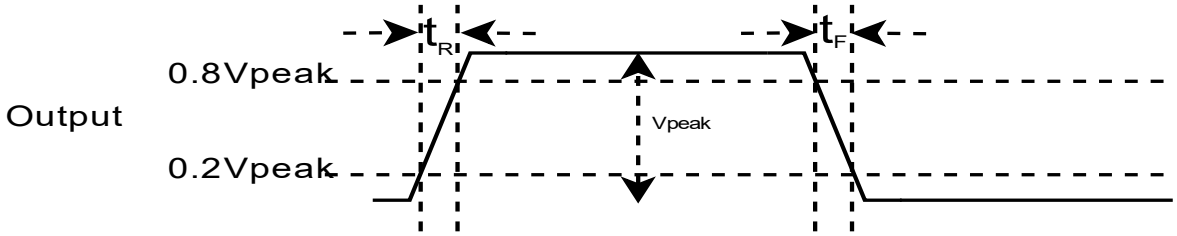


Figure 28 Parameter definitions related to rise and fall times

5 Hot Swap Recommendations

5.1 Introduction

Hot-swap is a term used to refer to the insertion and removal of a daughter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can be damaged.

5.2 Typical Differential Input Clock

For example, Figure 29 shows a typical LVPECL driver and differential input. If the power of the driver (VDDO) is turned on before the input supply (VDDI), there is a possibility that the input current could exceed the limit and damage diode D1.

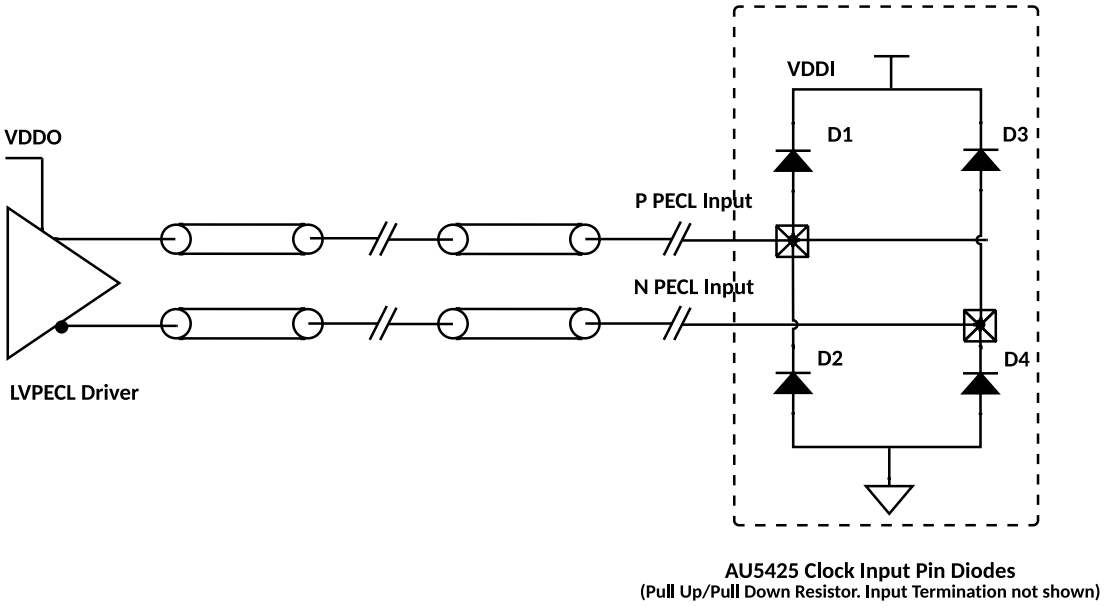


Figure 29 Typical input differential clock

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though it's not necessary, but if board space allows, some of the examples have an optional 100pf capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible

5.3 Input Clock Termination with Hot Swap Protection

5.3.1 LVPECL Termination Example

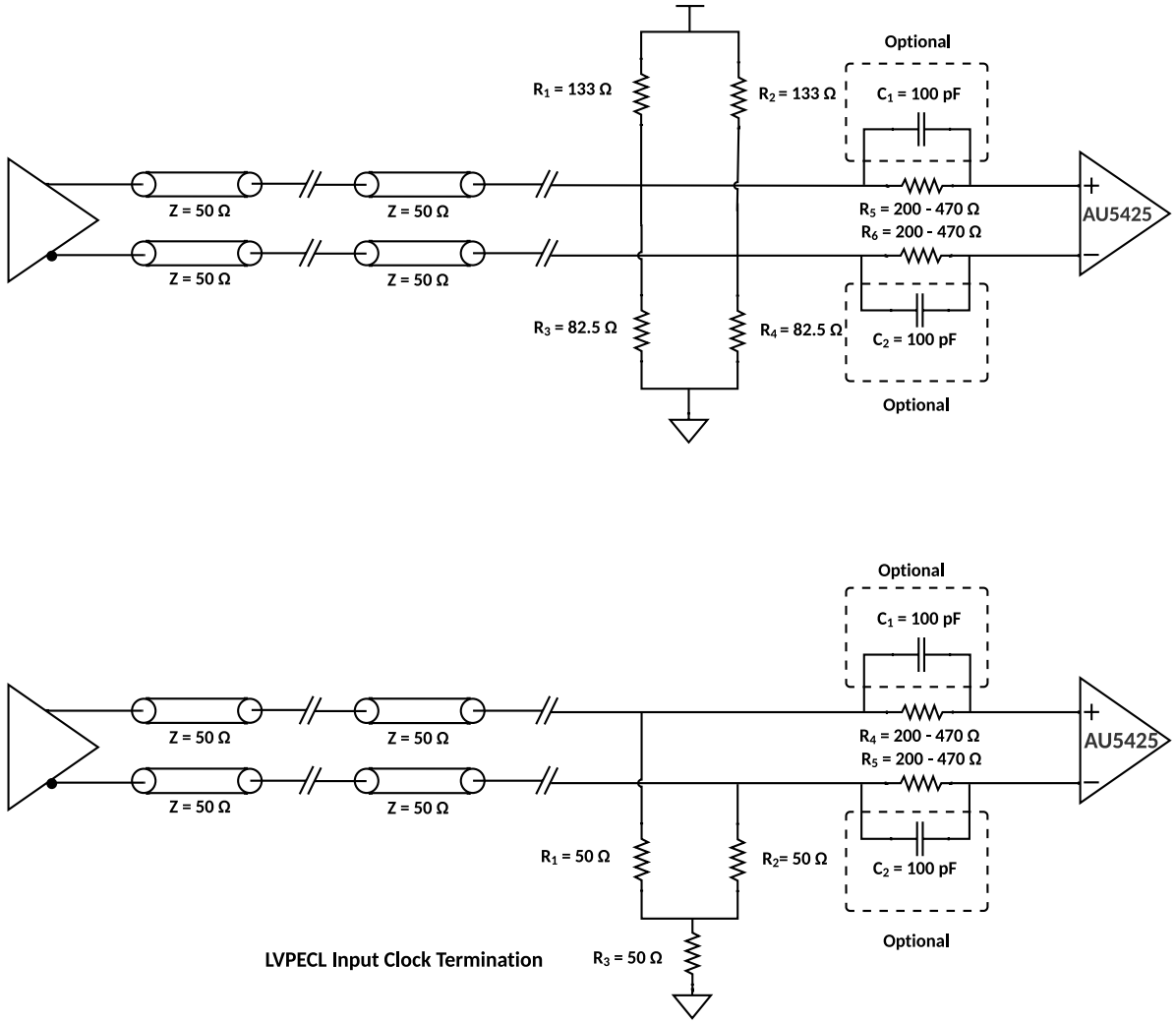


Figure 30 LVPECL termination with hot swap protection

5.3.2 LVDS Input Clock Termination Example

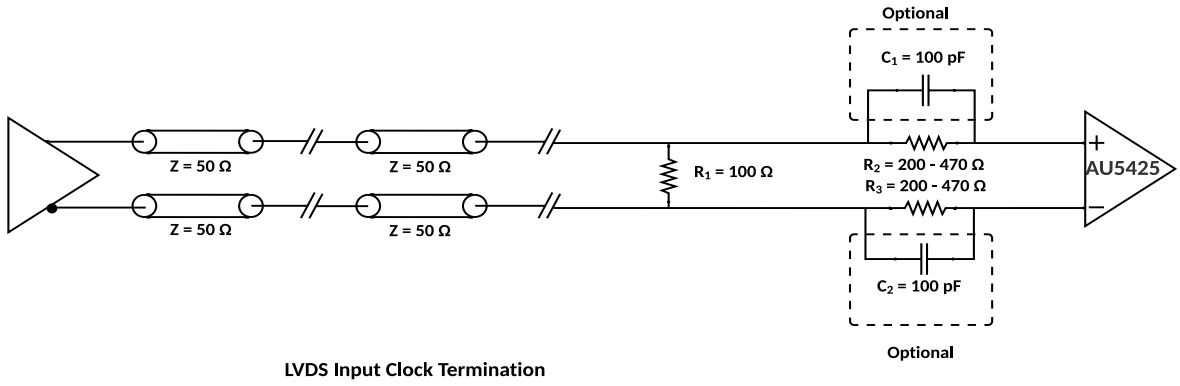


Figure 31 LVDS termination with hot swap protection

5.3.3 HCSL Input Clock Termination Example

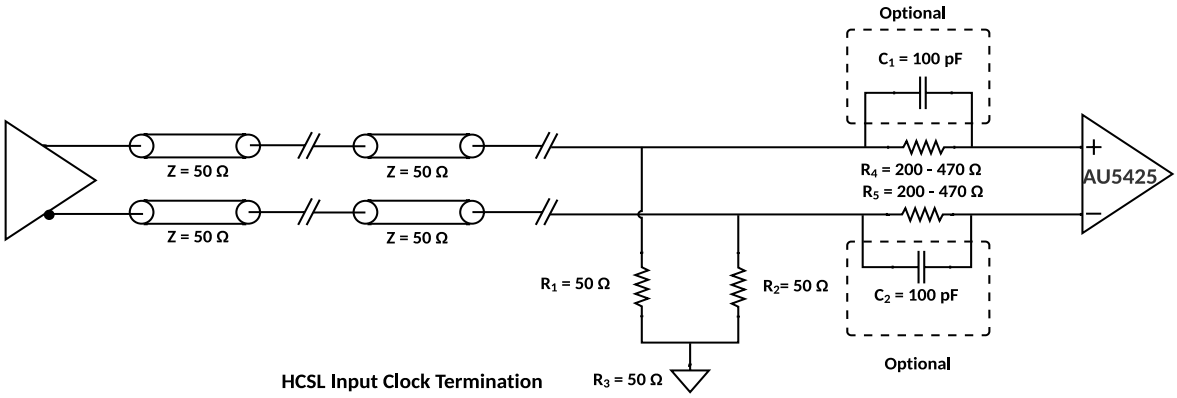


Figure 32 HCSL termination with hot swap protection

5.3.4 LVCMOS Input Clock Termination with Hot Swap Protection

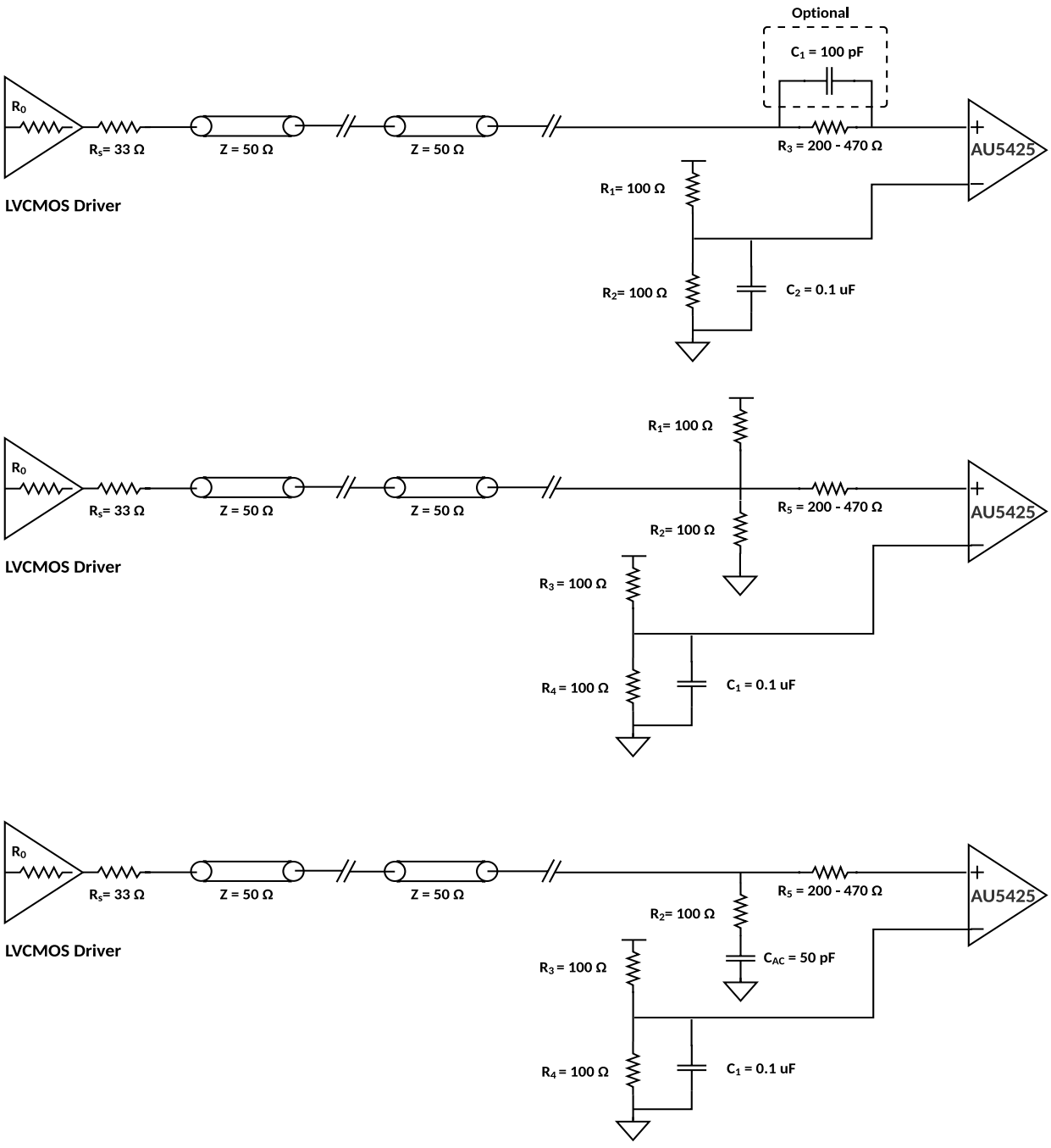


Figure 33 LVCMOS Input Clock Termination with Hot Swap Protection

5.4 LVCMOS Output Clock Termination with Hot Swap Protection

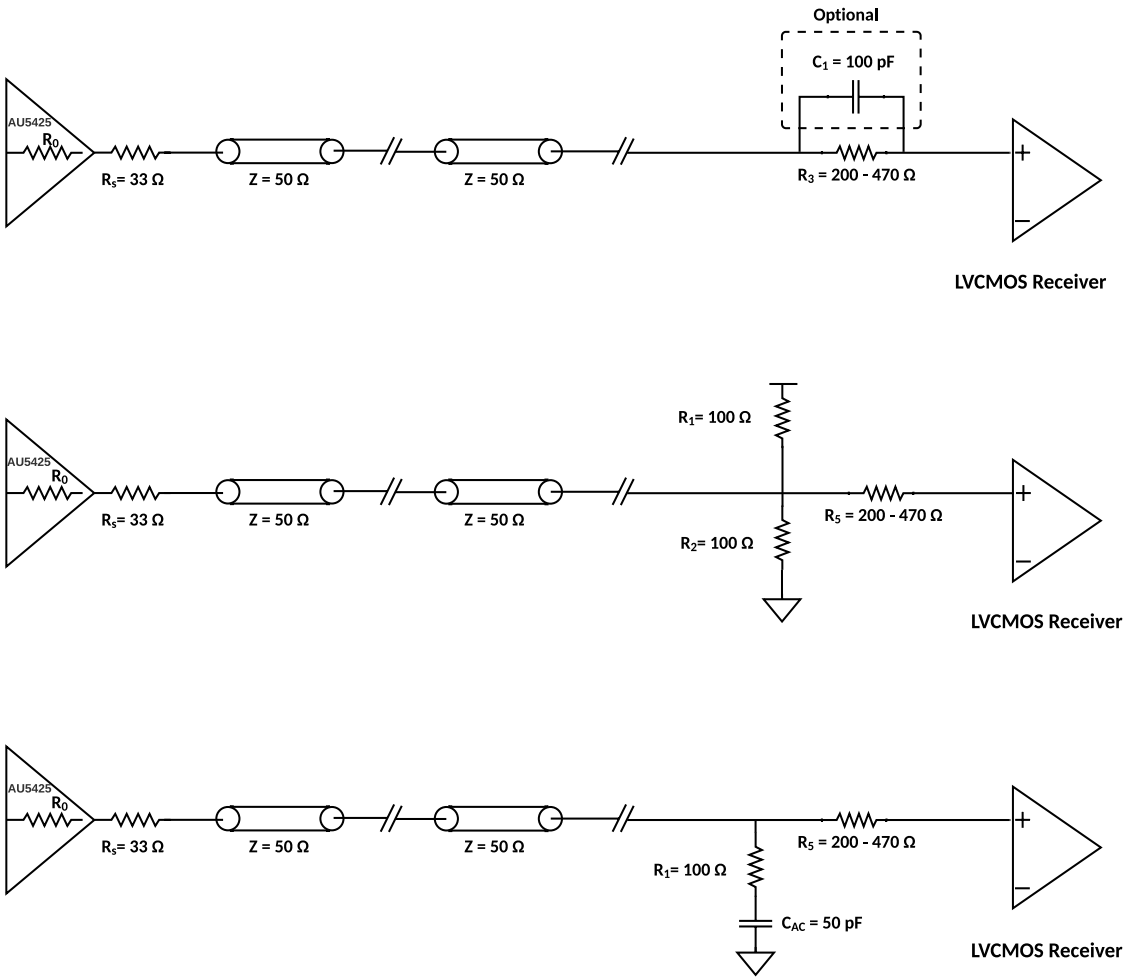


Figure 34 Different types of LVCMOS output clock termination with hot swap protection

6 Operation in Multiple V_{DDO} Supply Domains

The V_{DDO} pins, 2 and 6 on the left side are shorted internally. These pins along with ODR $CLK_{OUT}0$ to $CLK_{OUT}1$ belong to a single supply domain. The V_{DDO} pins, 18 and 14 on the left side are shorted internally. These pins along with ODR $CLK_{OUT}2$ to $CLK_{OUT}4$ belong to a single supply domain. These two supply domains are totally independent of each other. Pin 2, 6 can be connected to say 3.3 V while pin 18, 14 can be connected to 1.8 V. In this example, $CLK_{OUT}0$ to $CLK_{OUT}1$ will be 3.3 V LVCMOS driver. $CLK_{OUT}2$ to $CLK_{OUT}4$ will be 1.8 V LVCMOS driver.

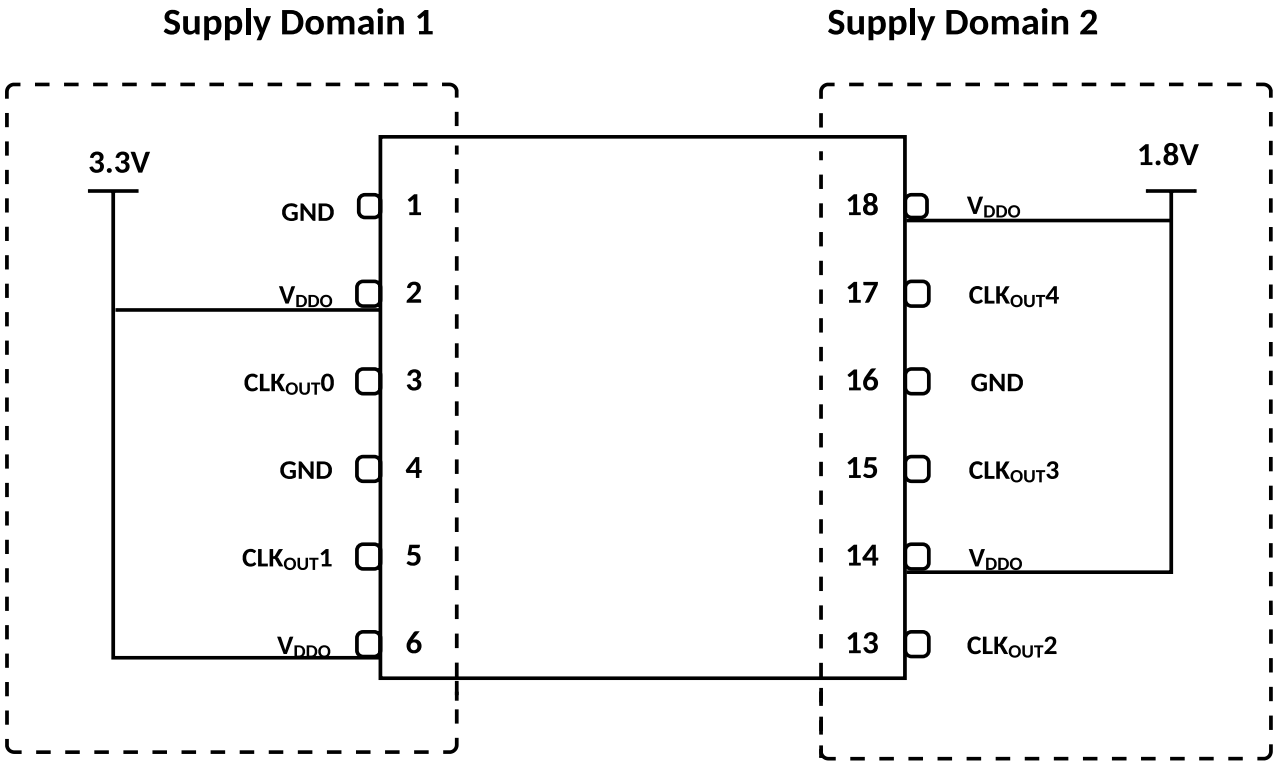
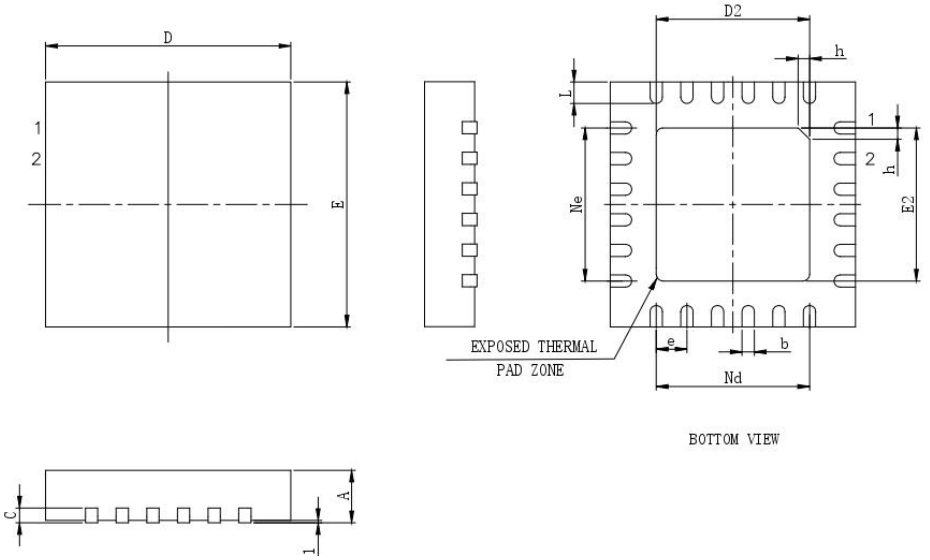


Figure 35 Example of multi supply operation of AU5425

Note:

7. Supply Domain 1 and Supply Domain 2 are independent of each other.

7 Package Information



SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0.70	0.75	0.80	
	0.80	0.85	0.90	4
	0.85	0.90	0.95	3
A1	—	0.02	0.05	
b	0.18	0.25	0.30	
c	0.18	0.20	0.25	
D	3.90	4.00	4.10	
D2	2.40	2.50	2.60	
e	0.50BSC			
Ne	2.50BSC			
Nd	2.50BSC			
E	3.90	4.00	4.10	
E2	2.40	2.50	2.60	
L	0.35	0.40	0.45	
h	0.30	0.35	0.40	

Figure 36 AU5425 24 Pin QFN Package Information

8 Ordering Information

Table 13 Ordering Information for AU5425

Ordering Part Number (OPN)	Marking	Package	Shipping Packaging	Temp Range
AU5425A-QMR(1)	AU5425A	24 QFN 4mm x 4mm	Tape and Reel	-40 °C to 85 °C
AU5425A-EVB	—	—	Evaluation Board	—

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering option.

9 Revision History

Table 14 Revision History

Version	Date	Description	Author
0.1	11th Nov 2020	AU5425 Datasheet	Aurasemi
0.2	27th May 2022	Section for driving OSC_IN with LVCMOS Driver (DC Coupled) is removed Updated the datasheet format	Aurasemi
1.0	1st Aug 2022	AU5425 Datasheet – Production Version Released	Aurasemi

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